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The Variability of 3D Total Ionizing dose Irradiation and NBTI Effects in Nanowire Gat-All-Around

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Abstract

The study of the radiation effects in microelectronic devices is essential in the space, avionic, and ground level applications affected by artificial and natural radiation environments, where the reliability is one of the most important requirements. The Total Ionizing Dose (TID) degradation mechanisms in several modern nanometer-scale technology nodes, we investigate in this paper work. The analysis of the TID mechanisms is focused on the evaluation of measurable effects affecting the threshold voltage of the devices and on the identification of the microscopical nature of the radiation-induced defects. Several transistors, based on Gate All Around (GAA) MOSFET nanowire structures of different manufacturers, have been simulated under ionizing radiation at several temperatures, bias configurations, annealing conditions, and transistor dimensions. Several different techniques, as NBTI static characterization, charge pumping and low frequency noise simulations as well as Technology Computer-Aided Design simulations, were used to identify location, density and energy levels of the radiation-induced defects. TID mechanisms have been studied following the technological evolution of the devices at nodes: 20 nm Si-based MOSFET, with SiO2/HfO2 gate dielectric. All results confirm the high TID tolerance of the thin gate oxide of nano scaled technologies, due to the reduced charge trapping in the gate dielectric.

Keywords: Degradation mechanisms; Transistors; Dielectric

Introduction

Electronic circuits are used in several application fields where different degrees of radiation tolerance may be required. The amount of radiation that semiconductor devices encounter during their lifecycle strongly depends on the radiation environment [1,2]. Typical applications within aggressive radiation environments are space and avionics systems, high energy physics experiments, nuclear power plants, medical diagnostic imaging and therapy, industrial imaging and material processing [3,4]. When operated in these environments, solid-state devices may be directly struck by photons, electrons, protons, neutrons or heavier particles, inducing an alteration of their electrical response, which can cause a temporarily or a permanently malfunction of the electronic

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system [5,6]

This work is focused on the TID mechanisms in modern semiconductor Field-Effect Transistors (FETs), i.e., MOSFETs. TID effects are induced by the Coulomb interaction between the device materials and the ionizing particles, which generate charges that can be collected and trapped in some sensitive part of the device. These charges are typically stuck in the insulator materials, and cause parametric shifts in the transistor electrical response [7].

The research on the basic degradation mechanisms is of great interest and essential to ensure the reliability of the electronic devices [8]. An extensive knowledge of the TID mechanisms allows to develop rad-hard circuits and design techniques to improve the tolerance of electronic circuits working in some specific applications, limiting failures and costs [9,10].

In order to fully interpret the simulation results, and thus to be able to predict the device responses in a variety of radiation environments, part 2 presents the state of the-art knowledge about TID mechanisms. While the methodology and results on the threshold voltage variability induced by discrete trap charges distributed in short-channel Si-NW FETs are discussed in physical models and analysis and results section. The radiation induced effects related to the gate oxide are analyzed in terms of generation, transport, and trapping of radiation induced charges in the oxides and along the oxide/semiconductor interface. New recent findings are discussed to underline the importance of TID degradation phenomena related to charge trapping in the shallow trench insulation and spacer dielectrics.

Basic Mechanism of the TID in MOSFET Devices

The TID is a cumulative effect based on the Coulomb interaction between the incident particle/photon and the electrons of the lattice of the material [11]. When a MOS device is irradiated with ionizing radiation, electron-hole (e-h) pairs are generated in the dielectrics. Electrons that escape initial recombination are typically swept out of an oxide under bias in picoseconds. Holes (positive charge) in SiO_2 have lower effective mobility than electrons and they are trapped in the insulator material [12]. Trapped charges in the oxide can change the electrical properties of the device, degrading its performance. The analysis of the TID effects is here focused on the TID mechanism related to the gate oxide, but it can typically be extended to other dielectric layers used in the semiconductor devices [13].

The device is irradiated with ionizing radiation with positive voltage at the gate terminal. The TID degradation in the gate oxide follow these stages:

- Ionization of the insulator with generation of e-h pairs.
- Partial recombination of e-h pairs.
- Hopping transport of holes through localized states.
- Deep hole trapping and border traps.
- Proton (H+) release and formation of interface traps.

With the shrink of the SiO_2 gate layers to thickness close to 1 nm, the TID effects related to the gate oxide have become increasingly less problematic in electronic devices for both digital and analog applications. In general, for thicknesses >10 nm, the flatband voltage shift per unit dose decreases with a trend proportional to t2ox. For thicknesses <10 nm, the decrease in hole trapping is much more rapid than the expected t^2ox dependence visible in thick oxide capacitors. This abrupt decrease in the hole trapping is related to the tunnelling electrons, which neutralize the trapped holes located within the ~3 nm of either the metal/oxide or oxide/semiconductor interfaces [10].

Similarly to the oxide charges, an abrupt reduction in the interface-trap density is visible at ultra-thin oxides <10 nm. Tunnelling

electrons from the metal/oxide or oxide/semiconductor interfaces neutralize the trapped hole in the oxide, avoiding the release of H+ responsible for the interface traps buildup. This bias dependence is in agreements with the generation and release of H+, which under positive bias are drifted toward the gate SiO_2/Si interface, where they can depassivate the Si-H bonds and generate interface traps [5,8].

The reduction of the TID effects related to gate oxide has a strong benefit the radiation response of MOSFET devices of modern technological nodes. However, TID effects have become less predictable with the advent of high-k gate materials and of alternative semiconductor materials and structures used by modern semiconductor industries. Indeed, the gate oxide is not the unique insulator layer in modern MOSFETs [7].

Radiation-induced degradation related to Shallow Trench Isolation (STI) is caused by positive charge buildup in the STI oxides, as shown in **FIG. 1**. Positive charge in the STI can significantly affect the radiation hardness of nanoscale transistors through two main degradation effects: increased radiation-induced standby currents and threshold voltage shifts in narrow-channel transistors, also called Radiation-Induced Narrow-Channel Effect (RINCE).

The causes of increased standby current are leakage paths created by the radiation-induced positive charge buildup in STI. The basic mechanisms for all STI-induced leakage phenomena are the same. Positive charge in STI oxides inverts the adjacent p-type Si regions, forming an inverted layer around the STI sidewalls. As the surface inverts, conducting paths are generated, markedly increasing the leakage current.

These leakage paths will cause an increase in static power supply current of an IC with radiation. As the radiation-induced charge buildup in the STI oxides is predominantly positive, its effect is usually most important for n-channel transistors.

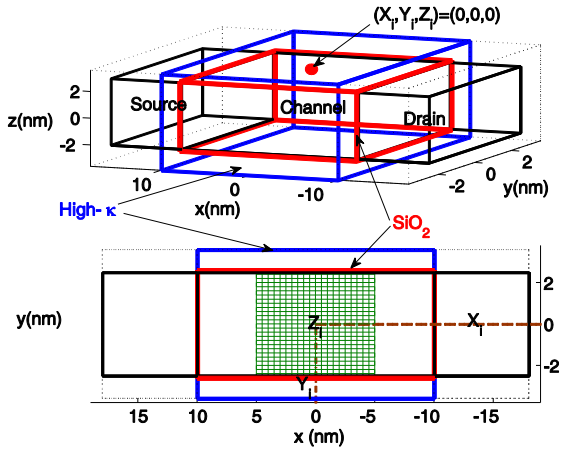

Fig. 1 **Schematic representation of a transistor with STI and the arrows indicate three possible leakage paths in technology nodes using STI. The first leakage path is at the edge of the bottom and top gate-oxide-high-κ transistor between the source and drain. The second leakage path is at the edge of the left and right gate-oxide-high-κ transistor between the source and drain. The third leakage path occurs between the n-type source and drain regions of nMOSFET and n-well of an adjacent niMOSFET.**

Physical Models

Numerical simulations are performed by self-consistently solving the 3-D Schrodinger and Poisson equations in the coherent transport regime in the presence of fixed charge centers trapped at the SiO2/high-κ dielectric interface.

In order to reduce the numerical burden the Coupled Mode Space (CMS) approach is used within the NEGF formalism [9]. According to the CMS approach the discrete electron correlation function reads:

$$G^{<}\left(i_1,i_2,j_1,j_2,k_1,k_2,E\right)=\sum_{n,m}G^{<}_{m_s}\left(i_1,i_2,n,m,E\right)\Phi^{n}_{i_1}\left(j_1,k_1\right)\Phi^{m^*}_{i_2}\left(j_2,k_2\right) \quad (1)$$

Where $\left\{\Phi^{n}_{i}\right\}n=1,2,\ldots,N_yN_z$ is the orthonormal set of eigen-functions solution of the 2-D Schrodinger problem for the i^{th} slice of the device, $G^{<}_{m_s}$ is the mode-space counter part of the real-space Green's function and Ny(Nz) indicates the number of discretization nodes along the y(z) confinement direction. The solution in the transverse plane is obtained assuming close boundary conditions with vanishing wave functions at the gateoxide interface. The Green's functions in the mode space are obtained as solution of the two of kinetic equations

$$\left[E-H_{m_s}-\sum\nolimits_{m_s}\right]G_{m_s}=I \quad (2)$$

$$G^{<}_{m_s}=G_{m_s}\sum\nolimits^{<}_{m_s}G^{\dagger}_{m_s}$$

Where $\sum^{<}_{m_s}$ and $\sum_{m_s}$ are the lesser-than and retarded self-energies describing the ideal infinite equipotential contacts, H_{m_s} is the mode-space Hamiltonian and I is the identity matrix, for every energy E, and then evaluating the real space electron density through the integral:

$$n_{i,j,k}=\frac{-ig_vg_s}{\Delta x}\int\frac{dE}{2\pi}\,G^{<}\left(\mathrm{i},\mathrm{i},\mathrm{j},\mathrm{j},\mathrm{k},\mathrm{k},E\right) \quad (3)$$

Where g_{vs} are the valley and spin degeneration coefficients, respectively.

The Poisson equation

$$\nabla\left(\varepsilon\left(\boldsymbol{r}\right)\nabla\phi\left(\boldsymbol{r}\right)\right)=\rho\left(\boldsymbol{r}\right) \quad (4)$$

is solved in the 3-D domain using the box-integration method, where ε(r) is the position dependent dielectric constant, ρ(r) is total charge density accounting for both electrons and fixed charges, and ϕ(r) is the self-consistent electrostatic potential.

Analysis and Results

In this simulation; applied source drain voltage is V_{GS} =400mV, 450mV and 500mV, and the temperature is T=300K. Consisting of a 20 nm undoped channel and 10nm SD regions nominally doped at $1020cm^{-3}$. The cross section of the devices is 5x5 nm^2, and the SiO_2 oxide and High-κ thickness are 0.2nm, 0.8nm respectively as shown in **FIG 1**. The first subband profile characteristics of such devices in the presence of a single trap charge located at the $\left(Si/SiO_2/high-\kappa\right)$ interfaces and at different positions along the (x-y-z) volume are shown in left of **FIG. 2**, where the on- turn curve of a clean device is plotted as the reference.

The manufacturer does not provide any information about the fabrication process, such as doping concentrations and materials used into the production of the 20 nm transistors. For this reason, the simulated device structure was designed on the basis of publicly available information and agreement with the simulation characterization of the pre-rad devices. For example, the high-k gate dielectric thickness was estimated by the gate capacitance of a n-channel varactor. Supposing a thickness of the SiO_2 layer of about 0.2 nm, the thickness of the HfO_2 layer results 0.8 nm.

Radiation induces charge trapping in oxide, border, and interface traps. The most efficient way to highlight the impact of each trap type is to simulate the electron concentration response in linear region. Right of **FIG. 2** shows schematically the typical electron

concentration curves of n-channel MOSFETs. The blow curves indicate the response before the irradiation. In Si MOSFETs with SiO_2 gate dielectric, radiation generates electron (negative charge) trapping in the gate oxide. The effect of oxide trapped charge is shown by the red curves, which evidence a parallel shift of the electron concentration. Interface traps have different effects on the responses of n-channel transistors, due to their amphoteric nature.

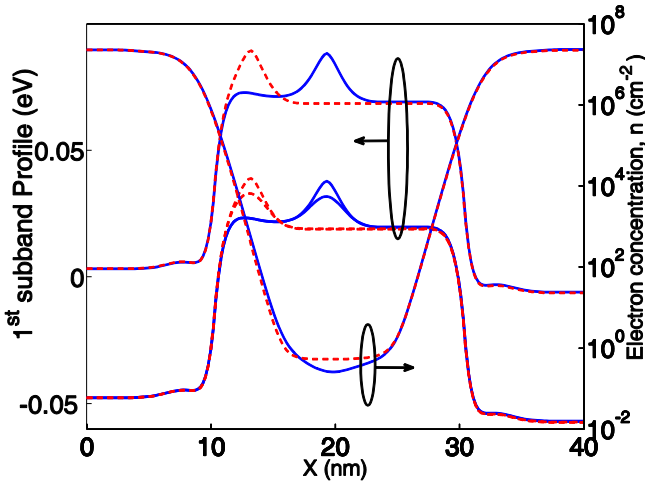

FIG. 2 **Top view of transistors along a horizontal cut-plane immediately below the gate oxide. The evolution of TID mechanisms are shown, related to STI charge buildup and the influence of the halo implantations in narrow MOSFETs biased in the linear region. The TID-induced effects are illustrated in long and short channel devices at high doses (~ 1-100 Mrad(SiO_2))**

The charge status of interface traps depends on the applied bias, which can trap or detrap the charge at the interface as the channel is swept from accumulation to inversion by the gate voltage. At mid-gap, interface-traps are neutral and do not impact the electron concentration curves.

Out of the mid-gap voltage, interface states influence the electron concentration characteristics by stretching the curves in the sub-threshold region. This is illustrated in **FIG. 2** by the blow and red curves, showing the stretch-out towards more positive values for nMOSFETs. The different sign in the trapped charge induces substantial differences in the overall radiation response of nMOSFET. While for an n-channel transistor interface traps are predominantly negative, causing positive threshold-voltage shifts. In nMOSFETs, the negative charge trapped in the interface traps can compensate partially or completely the effects of the oxide trapped holes. When the effects of the negative charge dominate, a rebound effect is typically visible in the threshold voltage.

The key difference between the interface and border traps is the rate at which the charge is exchanged between the trap and the substrate. Border traps are able to capture and emit electrons at slow time rates, typically ≤100 Hz. On the contrary, the time rates of interface traps is typically ≥1 kHz. Traps with emission/capture rates slower than the total time for a V_{gs} sweep are able to contribute just to hysteresis and threshold voltage shift, but not to the sub-threshold stretch out. On the contrary, border traps with emission/capture rates faster than the total time for a V_{gs} sweep are able to increase the sub-threshold stretch out.

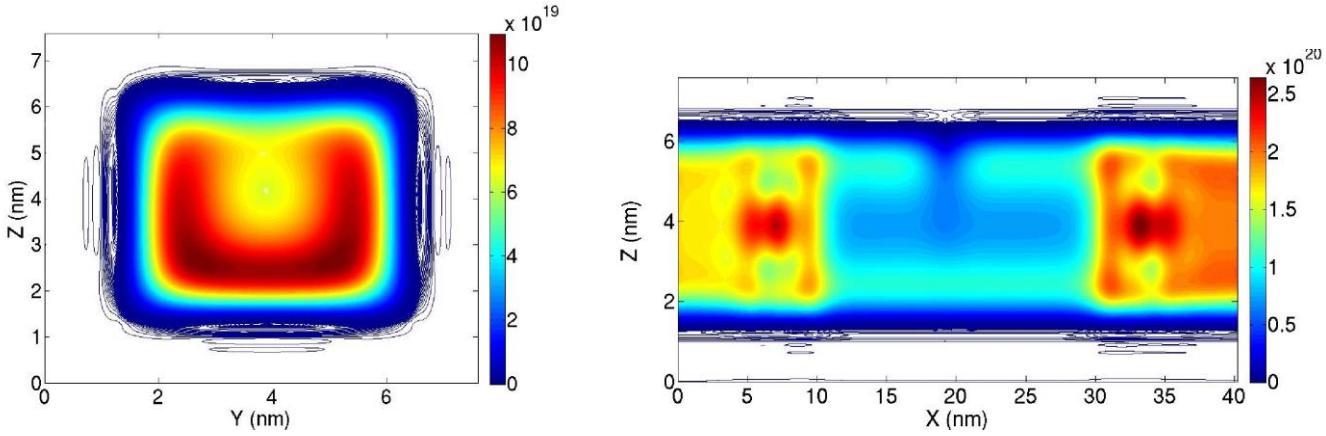

FIG. 3 **The 3D simulations of middle charge pumping of the 20 nm nMOSFETs. (top) The transversal section simulations are based on a 3D structure, implementing STI and halo regions. (bottom) In the third row, a cut plane at y=0.6 nm shows the doping concentrations in short and long channel MOSFETs. In the second row, cut plane at x=20 nm shows the delta space charge density, calculated as the difference of the space charge density between pre-rad and irradiated devices in short channel nMOSFETs.**

The radiation effects during the exposure are 3D simulated in bottom of **FIG. 3** which shows the electron density distribution under the source of the Lightly Doped Drains (LDD) extension of nMOSFET biased in linear region. Similar results are visible at the drain side. In top of **FIG. 3** show cross section electron density distribution under the channel extension of niMOSFET such that the middle charge influenced gradually of electron density distribution. Similarly in **FIG.4**, we show the radiation effects during the exposure such that the left position charge effect and 3D electron density distribution under the source LDD extension of nMOSFET biased in linear region. Similar results are visible at the drain side.

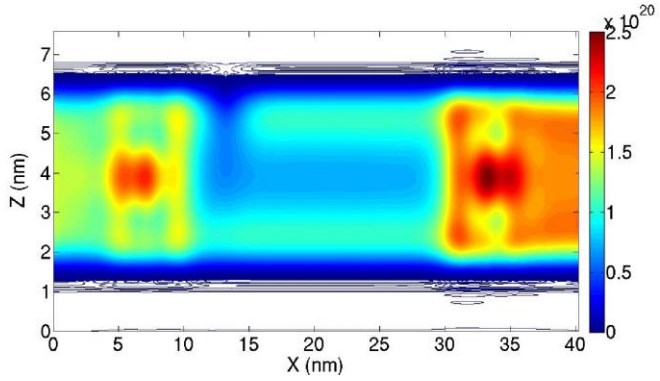

FIG. 4 **The 3D simulations of neighboring charge pumping of source of the 20 nm nMOSFETs. In the third row, a cut plane at y=0.6 nm shows the doping concentrations in short channel MOSFETs. In the second and first row, cut plane at x=20 nm shows the delta space charge density, calculated as the difference of the space charge density between pre-rad and irradiated devices in short channel nMOSFETs.**

FIG. 5, the variation of the threshold voltage Vth is plotted as a function of the dose for narrow and long channel transistors. Transistors are 3D simulated at room temperature in the linear region (Vds=0.4 V) at several irradiation steps up to 125

krad(SiO_2/high-κ) and after 24 hours of annealing at room temperature. The high sensitivity to Electro Static Discharge (ESD) discharges of core transistors combined with the numerous operations needed to carry out the high temperature annealing tests have limited the annealing simulations just to room temperature, and not to high temperature. nMOSFET shows positive Vth shift and gm degradation, which cause an increase of the maximum drain current of 29% at 125 krad(SiO_2/high-κ). Modest variation of leakage current is detected in the core nMOSFETs with an increase of Ioff of less than one order of magnitude. During room temperature annealing, the nMOSFET response is almost unchanged.

Thin-gate oxide transistors isolated by STI exhibit another TID effect in addition to deep STI channel leakage. During initial TID exposure (up to 20 krad), the charges in the STI are located higher, near the STI corner. This means that the gate is able to exert some control over the parasitic sidewall transistors. This effect, dubbed the sub threshold hump effect, is shown in the contrasting pre-rad and 20 krad curves of **FIG. 5**. However, as TID increases this effect is washed out by deep leakage within the STI.

It has been shown that the sub threshold hump effect is highly dependent on the MOSFETs structure. The high-voltage nMOSFET shows the worst hump effect followed by the I/O nMOSFET, which is finally followed by the core nFET. The oxide thickness at the STI corners plays an important role in this result. Figure 6 shows a cross-sectional diagram of the STI corner of the three different nMOSFET direction. And the thicker corner of the high-voltage device allows more charge to be trapped, thereby pronouncing the sub threshold hump effect. The sub threshold hump, as shown in **FIG. 5-6-7**, almost appears to be a shift in the threshold voltage of the device. As will be discussed later, high-voltage devices with thick STI corners could be an ideal candidate for the proposed 3D technique.

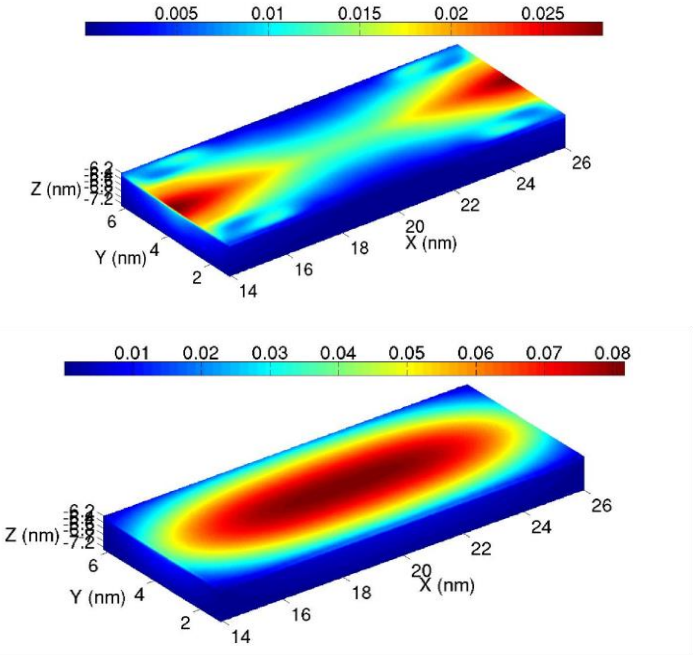

FIG. 5 **Radiation-induced threshold voltage shift at room temperature of different types of nMOSFETs direction (x,y,z) in the linear regime (VDS=0.40 V) irradiated up to 125 krad(SiO_2/high-κ) and for (top) VGS=0.20 V (bottom) VGS=0.60 V**

The sub threshold leakage current described previously is termed intra-device leakage. Inter-device leakage (leakage between neighboring devices) relies on charges trapped along the bottom of the STI. These trapped negative charges may invert n-type Si directly underneath them to form a leakage path between devices. However, recall that the electric field (i.e. proportional to the gate

voltage placed across the gate oxide) plays a large role in the susceptibility of charge trapping in the oxide. As the electric field increases, the number of electron-hole-pumping recombinations decreases, because the electrons and holes are pulled in opposite directions. There is a very low electric field at the bottom of the STI; therefore, charge trapping (and inter-device leakage) has been shown to be not as important as intra-device leakage.

FIG. 6 shows the current flow direction is perpendicular to the y-direction. The cross-section is cut between the source and the drain. The STI oxide is much thicker than the gate oxide and can trap negative charges under TID. These trapped charges can invert the active area abutting the STI and create a parasitic sidewall transistor that causes leakage current to flow from source to drain.

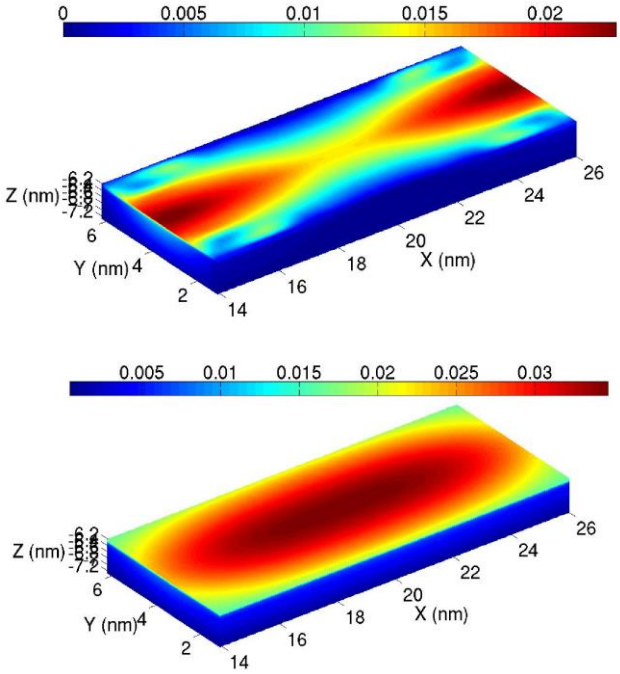

FIG. 6 **Radiation-induced threshold voltage shift at room temperature of different types of nMOSFETs direction (x,y,z) in the linear regime (VDS=0.45 V) irradiated up to 125 krad(SiO_2/high-κ) and for (top) VGS=0.20 V (bottom) VGS=0.60 V**

As discussed previously, TID has various deleterious effects on MOSFETs, especially nMOSFETs. The most important of these effects limits the ability of the nMOSFET to turn off. If the inverter has been exposed to a large amount of TID, when Vi (inverter gate) is a logic 'low' or zero volts there will still be leakage current through nMOSFET, N1, even though N1's VGS is zero. This increases the static power dissipation of digital circuits.

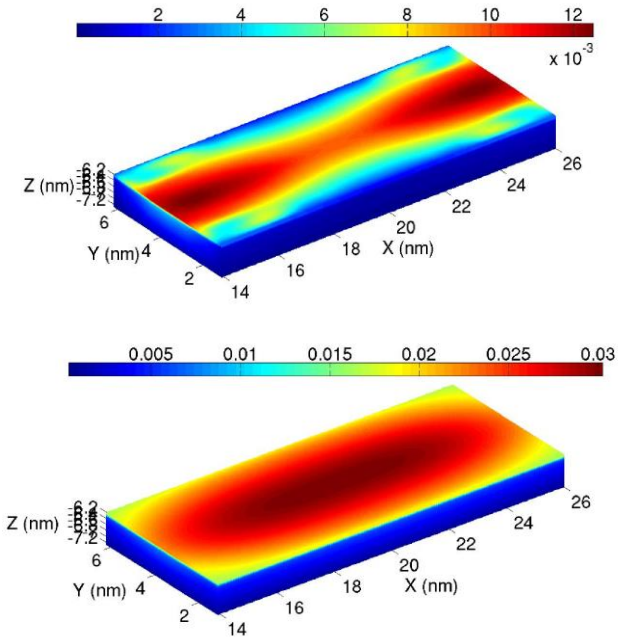

FIG. 7 **Radiation-induced threshold voltage shift at room temperature of different types of nMOSFETs direction (x,y,z) in the linear regime (VDS=0.50 V) irradiated up to 125 krad(SiO_2/high-κ) and for (top) VGS=0.20 V (bottom) VGS=0.60 V**

In addition, further increasing TID may cause the logic gate to fail entirely. **FIG. 7** shows the standard CMOS inverter and its transfer function under TID. The output, V_o, should be a logic 'high' or nearly VDD when the input is a logic 'low'. However as TID increases, the off-state resistance of the NFET decreases either through negative threshold voltage shift in thick-gate oxide NFETs or STI sidewall leakage in thin-gate oxide NFETs. Eventually, the output voltage will fall to a digitally indeterminate value and the digital circuit will fail.

The evolution with the average trap charge density Nt of the first tow statistical moments of the ΔVT probability distribution is finally plotted in Fig. 8. The behavior of the mean value (continue line), of the standard deviation (dashed line), at the large values of Nt is determined by the Poissonian distribution of the number of interface trap charges. In particular, we observe an almost linear increase of the mean threshold voltage shift, a power-law increase of the standard deviation with Nt.

nMOSFETs that support a large VGS voltage must have a gate oxide thick enough to prevent electric field breakdown. For older CMOS processes and high-voltage devices in newer processes, the gate oxide may be thicker than five nanometers to support the large VGS voltages. There are regions in the gate oxides that may trap negative charges that do not have a high probability of tunneling out of the oxide because they are too far from the interface. The most significant effect of ionizing radiation in these "thick-gate oxide" MOSFETs is threshold voltage variation. The most important failure mode of the MOSFETs in this case is the NMOS's transition from an enhancement-mode device to a depletion-mode device.

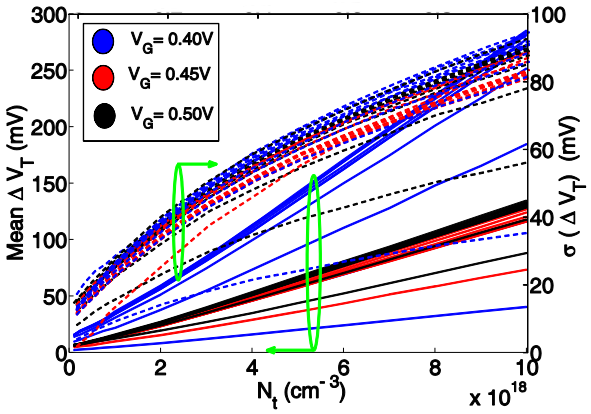

FIG. 8 **Mean value, standard deviation, of the threshold voltage shift probability due to discrete trap charges as functions of the interface trap density Nt.**

Finally the leakage current is a function of vertical location along the STI edge. As shown in **FIG.5-6-7**, the leakage current becomes worse further down in the STI. This is believed to be due to the positive gate bias during irradiation; the positive voltage repels the trapped electrons pushing them further into the STI. Because of the increased distance between the gate and the trapped charges, it is more difficult to control the transistor via the gate.

Conclusion

At ultra-high doses, the TID response of 20 nMOSFETs depends on channel width, channel length, and bias condition. Worst-case shifts are observed for both nMOSFETs and niMOSFETs irradiated at high gate voltage, due to increased charge yield in each, and to interface-trap formation in nMOSFETs at higher doses. DC and low frequency noise simulation indicate that negative charge trapping in the STI oxide leads to enhanced degradation in narrow channel transistors. At doses up to 100 Mrad(SiO_2), the dominant degradation mechanism is trapping of negative charges in the STI. At ultra-high doses, the effects of interface traps along the gate oxide and STI sidewalls become more significant. Low-frequency noise simulations show the presence of RTN in small devices and increased noise with dose, due primarily to charge trapping in the gate dielectric. Moreover, short-channel transistors show lower radiation-induced degradation than long channel ones. Indeed, modern CMOS technologies employ the halo implantations, highly doped bulk regions close to the extensions. In short channel transistors, the source and drain halo implantations can overlap each other, increasing the overall doping in the channel region. 3D simulations confirm the influence of the GAA doping concentration on the TID response. Higher bulk doping requires larger amount of charge to alter the carrier distribution, consequently mitigating the radiation-induced effects in short channel transistors. By simulations, we confirm that the channel-length dependence is associated with the halo implantations, which fortuitously increase the radiation tolerance of modern CMOS devices.

REFERENCES

1. Watanabe K, Kato M, Okabe T, et al. Radiation effects of double layer dielectric films. IEEE Trans. Nucl. Sci. 1986;33(6):1216-22.
2. Esqueda IS. The impact of stress-induced defects on MOS electrostatics and short-channel effects. Solid-State Electronics. 2015 Jan 1;103:167-72.

3. Boesch HE, McLean FB, McGarrity JM, et al. Role transport and charge relaxation in irradiated SiO2 MOS capacitors. IEEE Trans. Nucl. Sci. 1975;22(6):2163-7.
4. Gerardin S, Bagatin M, Cornale D, et al. Enhancement of transistor-to-transistor variability due to total dose effects in 65-nm MOSFETs. IEEE Trans. Nucl. Sci. 2015;62(6):2398-403.
5. Binder D, Smith EC, Holman AB. Satellite anomalies from galactic cosmic rays. IEEE Trans. Nucl. Sci. 1975;22(6):2675-80.
6. Fleetwood DM. Total ionizing dose effects in MOS and low-dose-rate-sensitive linear-bipolar devices. IEEE Trans. Nucl. Sci. 2013;60(3):1706-30.
7. Schwank JR, Shaneyfelt MR, Dodd PE. Radiation hardness assurance testing of microelectronic devices and integrated circuits: Radiation environments, physical mechanisms, and foundations for hardness assurance. IEEE Trans. Nucl. Sci. 2013;60(3):2074-100.
8. Schwank JR, Shaneyfelt MR, Fleetwood DM, et al. Radiation effects in MOS oxides. IEEE Trans. Nucl. Sci. 2008;55(4):1833-53.
9. Bekaddour A, Pala MG, Chabane-Sari NE, et al. Deterministic method to evaluate the threshold voltage variability induced by discrete trap charges in Si-nanowire FETs. IEEE trans. electron devices. 2012;59(5):1462-7.
10. Oldham TR, McLean FB. Total ionizing dose effects in MOS oxides and devices. IEEE trans. nucl. sci. 2003;50(3):483-99.
11. Fossum ER, Hondongwa DB. A review of the pinned photodiode for CCD and CMOS image sensors. IEEE J. electron devices soc. 2014.
12. McLean FB, Boesch Jr HE, Oldham TR. Electron-hole generation, transport and trapping in SiO 2. InIonizing radiation effects in MOS devices and circuits 1989.
13. McLean FB, Ausman Jr GA, Boesch Jr HE, et al. Application of stochastic hopping transport to hole conduction in amorphous SiO2. J. Appl. Phys. 1976;47(4):1529-32.